REMARKS

Claims 1-15 are pending in the present application.

This Amendment is in response to the Office Action mailed November 20, 2000. In the Office Action, the Examiner rejected Claims 1-15 under 35 U.S.C. § 103. Applicant has, amended Claims 1, 3 and 5. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

I. REJECTIONS UNDER 35 U.S.C. § 103(a)

In the Office Action, the Examiner rejected Claims 1-9 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,625,570 issued to Vizireanu et al. ("Vizireanu"). The Examiner rejected Claims 10-15 under 35 U.S.C. § 103(a) as being unpatentable over Vizireanu and in view of U.S. Patent No. 5,273,050 issued to Schaus et al. ("Schaus"). Applicants respectfully traverse the rejections for the following reasons.

Vizireanu discloses a system for inserting individualized audio segments into prerecorded video media. Audio segments are simultaneously inserted into respective video tapes (Vizireanu, Col. 12, lines 3-4). Upon completion of the simultaneous insertion, the VTR is put in stop mode and the VTR units are signaled to eject (Vizireanu, Col. 16, lines 23-35).

Schaus discloses an electrocardiographic (ECG) system with multiple cassette loader. The multiple cassette loader is used to insert tapes into cassette player and to retrieve and restack ejected tapes from cassette player after they have been read (Schaus, Col. 3, lines 27-30).

Vizireanu and Schaus, taken alone or in combination, do not disclose, suggest, or render obvious:

1) a plurality of seminconductor memory banks accessible to first and second processors for read and write operations;

2) storing subsets of audio data corresponding to different groups of audio channels.

Applicants maintain the same arguments as presented in the previous response. In addition, Applicants contend that Vizireanu and Schaus do not disclose, suggest, or render obvious storing subsets of audio data corresponding to different groups of audio channels. Vizireanu merely teaches audio segments are simultaneously inserted into respective video tapes (Vizireanu, Col. 12, lines 3-4).

The Examiner contended that it would have been obvious to one of ordinary skilled in the art to substitute the video tape recorders in Vizireanu with semicondctor memories. However, semiconductor memories were clearly known by Vizireanu, as indicated by the use of a computer with 4 MB RAM (Vizireanu, Col. 7, lines 28-35). Despite this obvious knowledge, Vizireanu did not use semiconductor memories in place of the VTR. This fact clearly shows that Vizireanu's teachings on the use of the array of VTR are not applicable for semiconductor memories because the objective is to insert audio segments into a VTR. In other words, there is no motivation to combine Vizireanu with Schaus, or with official notice.

Furthermore, the Examiner failed to show that the audio server card can function as a processor, which can perform a read and write operation.

Therefore, Applicants believe that independent Claims 1, 5 and their respective dependent Claims are distinguishable over the cited prior art references. Accordingly, Applicants respectfully request the rejections under 35 U.S.C. § 103(a) be withdrawn.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Three Times Amended) A method [for allocating real-time audio data from a first plurality of audio channels in a system having a first processor and a second processor, the method] comprising:

providing a [second] plurality of memory banks of semiconductor memory devices, each memory bank being accessible to [the] first and second processors for operations selected from the group comprising read and write operations; and

storing subsets of [said] audio data from a plurality of audio channels in the [second] plurality of memory banks, the subsets corresponding to different groups of the audio channels.

3. (Twice Amended) The method of claim 1 wherein the [second] plurality of memory banks includes two memory banks.

5. (Three Times Amended) A system [having first and second buses for processing real-time audio data from a first plurality of audio channels, the system] comprising:

first and second buses;

a first processor and a second processor coupled to said first and second busses, respectively; and

a [second] plurality of memory banks of semiconductor memory devices coupled to said first and second buses for storing said audio data, said [second] plurality of memory banks being accessible to the first and second processors for operations selected from the group comprising read and write operations, said [second] plurality of memory banks storing subsets of audio data from a plurality of audio channels, said subsets corresponding to different groups of the audio channels.

CONCLUSION

In view of the amendments and remarks made above, it is respectfully submitted that the pending claims are in condition for allowance, and such action is respectfully solicited.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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THINH V. NGUYEN
Reg. No. 42,034

12400 Wilshire Boulevard, Seventh Floor
Los Angeles, California 90025
(714) 557-3800

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on: January 19, 2001.

Rose Dunne — *Date* 01/19/01